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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/597,996	08/15/2006	Radu Catalin Surdeanu	NL04 0166 US1	8935
65913	7550	01/05/2010		
NXP, B.V. NXP INTELLECTUAL PROPERTY & LICENSING M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER TRAN, TRANG Q	
			ART UNIT 2811	PAPER NUMBER
			NOTIFICATION DATE 01/05/2010	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary**Application No.**

10/597,996

Applicant(s)

SURDEANU ET AL.

Examiner

TRANG Q. TRAN

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 September 2009.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 and 5-12 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-3, 5-12 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 15 August 2006 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/21/2009 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pellerin (WO 02/075781 A2) in view of Krivokapic (US 6,888,198).

Re. claim 1, Figs. 2A-2D of Pellerin disclose a semiconductor device comprising a silicon-containing semiconductor body (30) with a surface, which semiconductor body (30) is provided, near the surface thereof, with a transistor comprising: a gate (46) situated at the surface and having a side wall spacer (52) on either side of the gate (as seen in Fig. 2D), and further comprising, on either side of the gate (46), a diffusion

region (44) formed in the semiconductor body (30), at least one diffusion region (44+extension implant region 46) being provided at the surface of the semiconductor body (30) with a silicide region (50), characterized in that the silicide region (50) extends along the surface of the semiconductor body (30) and continues for more than 10 nm (Pg. 6, lines 18-19 of Pellerin discloses side wall spacer 52 having thickness (53) from 20 nm to 100 nm which overlaps with the silicide region; therefore Pellerin discloses the silicide region (50) continues for more than 10 nm under the sidewall spacer) under the side wall spacer (52).

Pellerin discloses the semiconductor device as claimed in claim 1, characterized in that the side wall spacer (52) has a shaped (as seen Fig. 2) and comprises a first portion, which borders on the gate and extends substantially perpendicularly with respect to the surface of the semiconductor body, and a second portion which extends along the surface of the semiconductor body (as seen in Fig. 2D).

However, Pellerin does not disclose the following limitation whereas Fig. 1 of Krivokapic teaches it is known in the art to provide a side wall spacer (as a oxide liner) is L-shaped.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the L-shape of the side wall of Krivokapic in Pellerin, order to achieve the device properties.

Furthermore, the change in shape of the the side wall spacer was a matter of choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the particular configuration of the side wall spacer was

significant. See *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Re. claim 2, Pellerin and Krivokapic disclose the semiconductor device as claimed in claim 1, Pellerin further discloses characterized in that the silicide region (50) contains a metal (see pg. 5, lines 39-40) which, in the silicide region formed, has a higher diffusion rate than silicon (see claim 3 below for claimed material).

Re. claim 3, Pellerin and Krivokapic disclose the semiconductor device as claimed in claim 2, Pellerin further discloses characterized in that the metal is selected from the group comprising nickel (Ni), platinum (Pt) (see pg. 5, lines 39-40).

Re. claim 5, Pellerin and Krivokapic disclose teaches semiconductor device as claimed in claim 1, however Pellerin and Krivokapic may not explicitly teach the second portion of the L-shaped side wall spacer has a thickness, measured in a direction perpendicular to the surface of the semiconductor body, of maximally 40 nm.

According to MPEP § 2144.04(IV)(A): In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide certain measurement, since it has been held that discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233; *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980); *In re Huang*, 100 F.3d 135, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996).

Re. claim 6, Pellerin and Krivokapic disclose the semiconductor device as claimed in claim 1, however Pellerin and Krivokapic may not explicitly teach whereas Fig. 1 of Krivokapic teaches it known in the art to provide an insulating layer (14) extends in the semiconductor body (12) in a direction parallel to the surface of the semiconductor body (12, as seen in fig. 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the insulating layer of Krivokapic in Pellerin, in order to define the active regions (Col. 1 lines 66-67, and Col. 2, line 1).

Re. claims 7-8, Pellerin and Krivokapic disclose the semiconductor device as claimed in claim 1, however Pellerin and Krivokapic may not explicitly teach whereas Fig. 1 and Col 2, lines 14-15 of Krivokapic discloses characterized in that the semiconductor body comprises a germanium component or strained-silicon layer (as seen in Col 2, lines 14-15).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the semiconductor body comprises a germanium

component or strained-silicon layer of Krivokapic in Pellerin, in order to improve the performance of the device.

Re. claim 9, Pellerin and Krivokapic disclose the semiconductor device as claimed in claim 1, Pellerin further discloses characterized in that the at least one diffusion region (44+extension implant region 46) comprises the silicide region (50) as seen in Figs. 2A-2D.

Re. claim 11, Pellerin and Krivokapic disclose the semiconductor device as claimed in claim 1, Pellerin further discloses characterized in that the silicide region (50) is completely below the side wall spacer (52).

Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pellerin in view of Yang et al. (US 2003/0162359).

Re. claim 10, Pellerin and Krivokapic disclose discloses the semiconductor device as claimed in claim 1, Pellerin further discloses characterized in that the at least one diffusion region comprises a diffusion region extension (extension implant region 46),

However Pellerin and Krivokapic disclose may not explicitly teach whereas Fig. 2 of Yang discloses the silicide region (260) comprising a silicide region extension (262), the silicide region extension falling completely within the diffusion region extension (242).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the silicide region extension of Yang in Pellerin; in order to decrease contact resistance.

Re. claim 12, Pellerin and Krivokapic disclose discloses the semiconductor device as claimed in claim 2, however Pellerin and Krivokapic disclose may not explicitly teach whereas Fig. 2 and ¶28 of Yang discloses characterized in that the silicide layer (260) comprising metal which is palladium (Pd).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the silicide layer having claimed material, in order for suitable material use.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide claimed material for silicide layer, since it have been held to be within the general skill of a worker in the art to select a know material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416

Response to Arguments

Applicant's arguments with respect to claims above have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRANG Q. TRAN whose telephone number is (571)270-3259. The examiner can normally be reached on Mon - Thu (9am-5pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. Q. T./
Examiner, Art Unit 2811
/Cuong Q Nguyen/
Primary Examiner, Art Unit 2811